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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,185	03/06/2002	Raymond J. Beffa	3037.10US (95-1074.10)	1655

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EXAMINER	
RODRIGUEZ, JOSEPH C	

ART UNIT	PAPER NUMBER
3653	

NOTIFICATION DATE	DELIVERY MODE
01/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	10/092,185	BEFFA, RAYMOND J.	
	Examiner	Art Unit	
	Joseph C. Rodriguez	3653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 March 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 12/12/07.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Here, Applicant has established an "enhanced reliability testing flag" and "a reliability testing flag" in claims 2 and 3 and it is unclear if these flags are the same, or otherwise. Examiner requests clarification and, in the interim, has interpreted the claim language as set forth below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shils et al. ("Shils")(US 4,510,673) in view of Moosa et al. ("Moosa")(US 5,822,218) and Jernigan (US 5,642,307).

Shils (Fig. 1) teaches a testing method for an integrated circuit comprising

establishing data for an integrated circuit device resulting from fabrication errors and manufacturing deviations from a manufacturing process for an integrated circuit device of a plurality of integrated circuit devices (col. 4, ln. 12-34; col. 6);

storing data associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires additional testing (col. 3-6 teaching inscribing ICs with unique code, test data, such as good/bad/or only partially usable, and manufacturing process data to assist with additional testing);

automatically reading the unique identification code of each integrated circuit device of the plurality of integrated circuit devices wherein each integrated circuit device of the plurality of integrated circuit devices forms a portion of a wafer (Fig. 1; col. 5),

accessing the data stored for the unique identification code of each integrated circuit device of the plurality of integrated circuit devices (Id.);

sorting the plurality of integrated circuit devices in accordance with whether the data indicates they are in need of further testing (Id. with fig. 1 showing placement of chips into different banks and different process steps for chips of different types); and

performing further testing for each integrated circuit device of the plurality of integrated circuit devices requiring further testing (Id. see "Failure Analysis" and "Rework" process steps).

Shils as set forth above thus teaches all that is claimed except for expressly teaching said data including an enhanced reliability test flag that explicitly determines the type of further testing to perform on the IC. Shils teaches storing test data (including

a good/bad parameter) and manufacturing data that assists in the selection of further testing, but does not explicitly teach that the good/bad parameter controls further testing. Moosa, however, teaches the establishing of a specific parameter (i.e., flag) that determines the type of reliability testing (Fig. 13-15; col. 3, 4, 8, 26 teaching developing reliability models and designing specific test structures based on said models). Jernigan also teaches the use of different processing parameters during further reliability testing (col. 1, ln. 50-60; col. 6-8). Thus, it would be obvious to one with ordinary skill in the art to modify the base reference with these prior art teachings to arrive at the claimed invention. The rationale for this obviousness determination can be found in the prior art itself as Moosa expressly teaches that this type of parameter based reliability modeling more accurately predicts IC failures (col. 5). The rational can also be found in the nature of the problem being solved. Here, Applicant is attempting to resolve the problem of more efficiently testing ICs. Shils and Jernigan solve this problem with the use of unique identification codes with manufacturing process data placed on the actual device and Moosa teaches sophisticated reliability modeling that develops a parameter (i.e., testing flag) and specific test structures based on the reliability model. In view of these prior art teachings, it is difficult to argue that one with skill in the art would not know to add the parameter/flag of Moosa to the prior art teachings of Shils to arrive at the claimed invention to achieve more efficient failure analysis. Further, the modification to arrive at the claimed invention would merely involve the substitution/addition of well-known elements with no change in their respective functions (i.e., addition of parameter and reliability model of Moosa to

process data developed by Shils and Jernigan). Moreover, the use of prior art elements according to their functions is a predictable variation that would yield predictable results, and thus cannot be regarded as a non-obvious modification when the modification is already commonly implemented in the prior art. Further, the prior art discussed and cited demonstrates the level of sophistication of one with ordinary skill in the art and that these modifications would be well within this skill level. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the invention of Shils for the reasons set forth above.

Conclusion

Any references not explicitly discussed above but made of record are considered relevant to the prosecution of the instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Joseph C Rodriguez** whose telephone number is **571-272-6942** (M-F, 9 am – 6 pm, EST). The Supervisory Examiner is Patrick Mackey, **571-272-6916**. The **Official** fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

The examiner's **UNOFFICIAL Personal fax number** is **571-273-6942.**

Further, information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available

through Private PMR only. For more information about the PAIR system, see

http://pair-direct.uspto.gov

Should you have questions on access to the Private PMR system, contact the Electronic Business Center (EBC) at **866-217-9197** (Toll Free).

Signed by Examiner /Joseph Rodriguez/

Jcr

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January 6, 2008